# **74AUP1G38**

# Low-power 2-input NAND gate (open drain) Rev. 01 — 20 October 2006

**Product data sheet** 

#### **General description** 1.

The 74AUP1G38 is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire  $V_{CC}$  range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V<sub>CC</sub> range from 0.8 V to 3.6 V.

This device is fully specified for partial Power-down applications using I<sub>OFF</sub>. The I<sub>OFF</sub> circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74AUP1G38 provides the single 2-input NAND gate with open-drain output. The output of the device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

#### **Features** 2.

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
  - ◆ JESD8-12 (0.8 V to 1.3 V)
  - ◆ JESD8-11 (0.9 V to 1.65 V)
  - ◆ JESD8-7 (1.2 V to 1.95 V)
  - ◆ JESD8-5 (1.8 V to 2.7 V)
  - ◆ JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114-D exceeds 5000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101-C exceeds 1000 V
- Low static power consumption;  $I_{CC} = 0.9 \mu A$  (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V<sub>CC</sub>
- I<sub>OFF</sub> circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



**74AUP1G38 NXP Semiconductors** 

Low-power 2-input NAND gate (open drain)

# **Ordering information**

#### Table 1. **Ordering information**

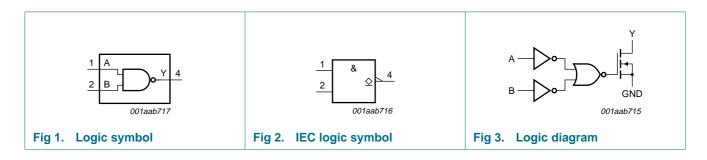
Type number	Package									
	Temperature range	Name	Description	Version						
74AUP1G38GW	–40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1						
74AUP1G38GM	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 $\times$ 1.45 $\times$ 0.5 mm	SOT886						
74AUP1G38GF	–40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 $\times$ 1 $\times$ 0.5 mm	SOT891						

## **Marking**

#### Table 2. Marking

Type number	Marking code
74AUP1G38GW	аВ
74AUP1G38GM	аВ
74AUP1G38GF	аВ

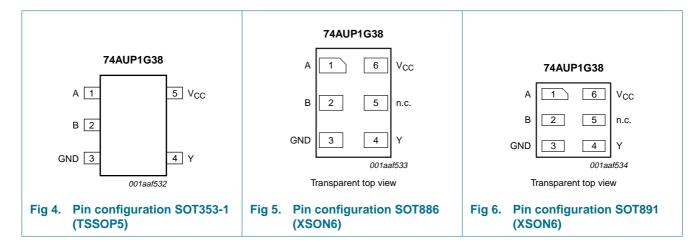
# 5. Functional diagram



Low-power 2-input NAND gate (open drain)

## 6. Pinning information

#### 6.1 Pinning



#### 6.2 Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5	XSON6	
A	1	1	data input A
В	2	2	data input B
GND	3	3	ground (0 V)
Υ	4	4	data output Y
n.c.	-	5	not connected
V <sub>CC</sub>	5	6	supply voltage

# 7. Functional description

Table 4. Function table[1]

Input		Output
Α	В	Υ
L	L	Z
L	Н	Z
Н	L	Z
Н	Н	L

<sup>[1]</sup> H = HIGH voltage level;

L = LOW voltage level;

Z = high-impedance OFF state.

#### Low-power 2-input NAND gate (open drain)

## 8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
I <sub>IK</sub>	input clamping current	$V_I < 0 V$	-	-50	mA
$V_{I}$	input voltage		[ <u>1]</u> –0.5	+4.6	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-	-50	mA
Vo	output voltage	Active mode and Power-down mode	<u>[1]</u> –0.5	+4.6	V
Io	output current	$V_O = 0 V \text{ to } V_{CC}$	-	+20	mA
I <sub>CC</sub>	supply current		-	+50	mA
$I_{GND}$	ground current		-	-50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C} \text{ to } +125  ^{\circ}\text{C}$	[2] _	250	mW

<sup>[1]</sup> The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		0.8	3.6	V
$V_{I}$	input voltage		0	3.6	V
$V_{O}$	output voltage	Active mode and Power-down mode	0	3.6	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	0	200	ns/V

## 10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$T_{amb} = 2$	5 °C					
$V_{IH}$	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	$0.70 \times V_{CC}$	-	-	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	V
		$V_{CC}$ = 2.3 V to 2.7 V	1.6	-	-	V
		$V_{CC}$ = 3.0 V to 3.6 V	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		$V_{CC} = 0.9 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	V
		$V_{CC}$ = 2.3 V to 2.7 V	-	-	0.7	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	-	0.9	V

<sup>[2]</sup> For TSSOP5 packages: above 87.5 °C the value of P<sub>tot</sub> derates linearly with 4.0 mW/K. For XSON6 packages: above 45 °C the value of P<sub>tot</sub> derates linearly with 2.4 mW/K.

## Low-power 2-input NAND gate (open drain)

**Table 7. Static characteristics** ...continued
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>OL</sub>	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O$ = 20 $\mu$ A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	0.1	V
		$I_{O} = 1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	-	-	$0.3 \times V_{CC}$	V
		$I_{O} = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.31	V
		$I_{O} = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.31	V
		$I_{O} = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.31	V
		$I_{O} = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.44	٧
		$I_{O} = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.31	٧
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.44	٧
l <sub>l</sub>	input leakage current	$V_I$ = GND to 3.6 V; $V_{CC}$ = 0 V to 3.6 V	-	-	±0.1	μΑ
I <sub>OFF</sub>	power-off leakage current	$V_I$ or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.2	μΑ
$\Delta I_{OFF}$	additional power-off leakage current	$V_1$ or $V_0 = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.2	μΑ
lcc	supply current	$V_I$ = GND or $V_{CC}$ ; $I_O$ = 0 A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	0.5	μΑ
$\Delta I_{CC}$	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	40	μΑ
Cı	input capacitance	$V_{CC} = 0 \text{ V to } 3.6 \text{ V; } V_I = \text{GND or } V_{CC}$	-	8.0	-	pF
Co	output capacitance	output enabled; $V_O = GND$ ; $V_{CC} = 0 V$	-	1.7	-	рF
		output disabled; $V_O = GND$ ; $V_{CC} = 0 V$	-	1.1	-	pF
T <sub>amb</sub> = -	40 °C to +85 °C					
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	$0.70 \times V_{CC}$	-	-	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	٧
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	$0.35 \times V_{CC}$	٧
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
V <sub>OL</sub>	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O$ = 20 $\mu$ A; $V_{CC}$ = 0.8 V to 3.6 V	-	-	0.1	V
		$I_{O} = 1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	-	-	$0.3 \times V_{CC}$	V
		$I_{O} = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.37	٧
		$I_{O} = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.35	V
		$I_{O} = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.33	V
		$I_O = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.45	V
		$I_{O} = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.33	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.45	V
l <sub>l</sub>	input leakage current	$V_I$ = GND to 3.6 V; $V_{CC}$ = 0 V to 3.6 V	-	-	±0.5	μΑ
l <sub>OFF</sub>	power-off leakage current	$V_{I}$ or $V_{O} = 0 \text{ V}$ to 3.6 V; $V_{CC} = 0 \text{ V}$	-	-	±0.5	μΑ
$\Delta I_{OFF}$	additional power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V; V <sub>CC</sub> = 0 V to 0.2 V	-	-	±0.6	μΑ

## Low-power 2-input NAND gate (open drain)

 Table 7.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I <sub>CC</sub>	supply current	$V_I = GND \text{ or } V_{CC}; I_O = 0 \text{ A};$ $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$			0.9	μΑ
$\Delta I_{CC}$	additional supply current	$V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	50	μΑ
T <sub>amb</sub> = -	40 °C to +125 °C					
$V_{IH}$	HIGH-level input voltage	V <sub>CC</sub> = 0.8 V	$0.75 \times V_{CC}$	-	-	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	$0.70 \times V_{CC}$	-	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.6	-	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	V <sub>CC</sub> = 0.8 V	-	-	$0.25 \times V_{CC}$	V
		V <sub>CC</sub> = 0.9 V to 1.95 V	-	-	$0.30 \times V_{CC}$	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	-	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	-	0.9	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$I_O$ = 20 $\mu$ A; $V_{CC}$ = 0.8 $V$ to 3.6 $V$	-	-	0.11	V
		$I_O = 1.1 \text{ mA}; V_{CC} = 1.1 \text{ V}$	-	-	$0.33 \times V_{CC}$	V
		$I_O = 1.7 \text{ mA}; V_{CC} = 1.4 \text{ V}$	-	-	0.41	V
		$I_O = 1.9 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.39	V
		$I_{O} = 2.3 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.36	V
		$I_O = 3.1 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.50	V
		$I_{O} = 2.7 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.36	V
		$I_{O} = 4.0 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.50	V
II	input leakage current	$V_I$ = GND to 3.6 V; $V_{CC}$ = 0 V to 3.6 V	-	-	±0.75	μΑ
I <sub>OFF</sub>	power-off leakage current	$V_I$ or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V	-	-	±0.75	μΑ
$\Delta I_{OFF}$	additional power-off leakage current	$V_1$ or $V_O = 0$ V to 3.6 V; $V_{CC} = 0$ V to 0.2 V	-	-	±0.75	μΑ
I <sub>CC</sub>	supply current	$V_I = GND \text{ or } V_{CC}; I_O = 0 \text{ A};$ $V_{CC} = 0.8 \text{ V to } 3.6 \text{ V}$	-	-	1.4	μΑ
$\Delta I_{CC}$	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A}; V_{CC} = 3.3 \text{ V}$	-	-	75	μΑ

Low-power 2-input NAND gate (open drain)

# 11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 8

Symbol	Parameter	Conditions			25 °C		-40	°C to +1	25 °C	Unit
				Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
C <sub>L</sub> = 5 pl	F				'					
t <sub>pd</sub>	propagation delay	A or B to Y; see Figure 7	[2]							
		$V_{CC} = 0.8 \text{ V}$		-	13.5	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		1.9	4.6	10.4	1.8	11.4	12.6	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		1.5	3.3	6.5	1.4	7.4	8.2	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		1.2	2.9	5.1	1.1	5.9	6.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.0	2.2	3.8	0.9	4.5	4.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		0.9	2.3	4.0	0.8	4.5	4.9	ns
C <sub>L</sub> = 10										
$t_{pd}$	propagation delay	A or B to Y; see Figure 7	[2]							
		$V_{CC} = 0.8 \text{ V}$		-	16.3	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		2.3	5.6	12.3	2.1	13.7	15.1	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		1.8	4.1	7.6	1.7	8.8	9.7	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		1.6	3.8	6.1	1.4	7.1	7.8	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.4	2.9	4.6	1.2	5.4	5.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.3	3.2	5.7	1.1	6.4	7.0	ns
C <sub>L</sub> = 15										
$t_{pd}$	propagation delay	A or B to Y; see Figure 7	[2]							
		$V_{CC} = 0.8 \text{ V}$		-	19.0	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		2.6	6.6	14.2	2.4	15.8	17.4	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		2.1	4.8	8.7	1.9	10.1	11.1	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		1.9	4.6	7.6	1.7	8.5	9.3	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		1.6	3.6	5.6	1.5	6.3	6.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		1.6	4.1	7.5	1.4	8.3	9.1	ns
$C_L = 30$										
$t_{pd}$	propagation delay	A or B to Y; see Figure 7	[2]							
		$V_{CC} = 0.8 \text{ V}$		-	27.0	-	-	-	-	ns
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		3.6	9.5	19.5	3.2	21.8	24.0	ns
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		2.9	7.0	11.5	2.6	13.6	15.0	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		2.6	7.0	12.1	2.3	13.3	14.6	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		2.4	5.4	8.9	2.1	9.9	10.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		2.3	6.5	12.7	2.1	13.9	15.3	ns

#### Low-power 2-input NAND gate (open drain)

 Table 8.
 Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V; for test circuit see Figure 8

Symbol	nbol Parameter Conditions			25 °C		-40	Unit			
				Min	Typ[1]	Max	Min	Max (85 °C)	Max (125 °C)	
$C_L = 5 pl$	F, 10 pF, 15 pF and	30 pF								
C <sub>PD</sub> power dissipation capacitance	•	$f_i = 1 \text{ MHz};$ $V_I = \text{GND to } V_{CC}$	[3]							
		$V_{CC} = 0.8 \text{ V}$		-	0.6	-	-	-	-	pF
		$V_{CC} = 1.1 \text{ V to } 1.3 \text{ V}$		-	0.7	-	-	-	-	pF
		$V_{CC} = 1.4 \text{ V to } 1.6 \text{ V}$		-	0.8	-	-	-	-	pF
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		-	0.9	-	-	-	-	pF
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		-	1.1	-	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		-	1.4	-	-	-	-	pF

<sup>[1]</sup> All typical values are measured at nominal V<sub>CC</sub>.

[3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

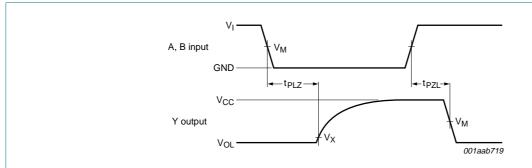
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N$  where:

 $f_i$  = input frequency in MHz;

 $V_{CC}$  = supply voltage in V;

N = number of inputs switching.

#### 12. Waveforms



Measurement points are given in Table 9.

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.

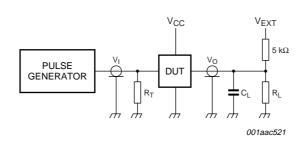
Fig 7. The data input (A or B) to output (Y) propagation delays

Table 9. Measurement points

Supply voltage	Input	Output				
V <sub>CC</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>			
0.8 V to 1.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.1 V			
1.65 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V <sub>OL</sub> + 0.15 V			
3.0 V to 3.6 V	$0.5 \times V_{\text{CC}}$	$0.5 \times V_{\text{CC}}$	V <sub>OL</sub> + 0.3 V			

<sup>[2]</sup>  $t_{pd}$  is the same as  $t_{PZL}$  and  $t_{PLZ}$ .

#### Low-power 2-input NAND gate (open drain)



Test data is given in Table 10.

Definitions for test circuit:

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

V<sub>EXT</sub> = External voltage for measuring switching times.

Fig 8. Load circuitry for switching times

#### Table 10. Test data

Supply voltage	Load		V <sub>EXT</sub>		
V <sub>CC</sub>	C <sub>L</sub>	R <sub>L</sub> [1]	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 k $\Omega$ or 1 M $\Omega$	open	GND	$2 \times V_{CC}$

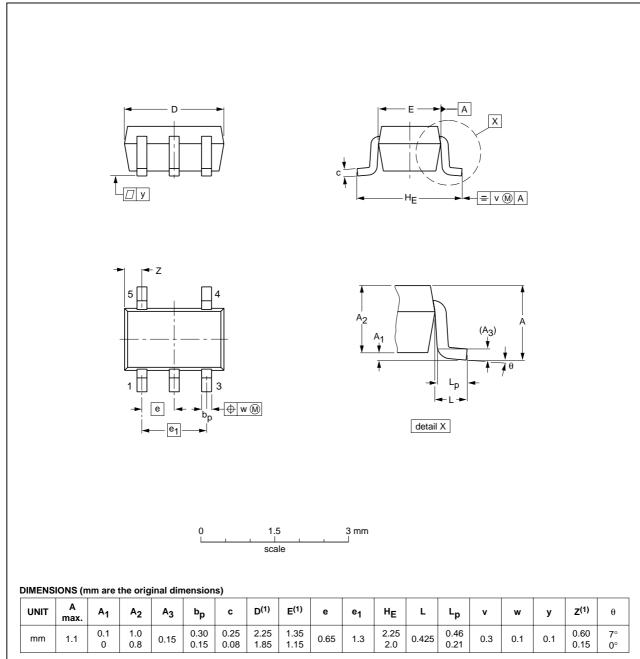
[1] For measuring enable and disable times  $R_L$  = 5  $k\Omega$ , for measuring propagation delays, setup and hold times and pulse width  $R_L$  = 1  $M\Omega$ .

#### Low-power 2-input NAND gate (open drain)

## 13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



#### Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE	REFERENCES			EUROPEAN	ISSUE DATE	
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT353-1		MO-203	SC-88A			<del>-00-09-01</del> 03-02-19

Fig 9. Package outline SOT353-1 (TSSOP5)

Low-power 2-input NAND gate (open drain)

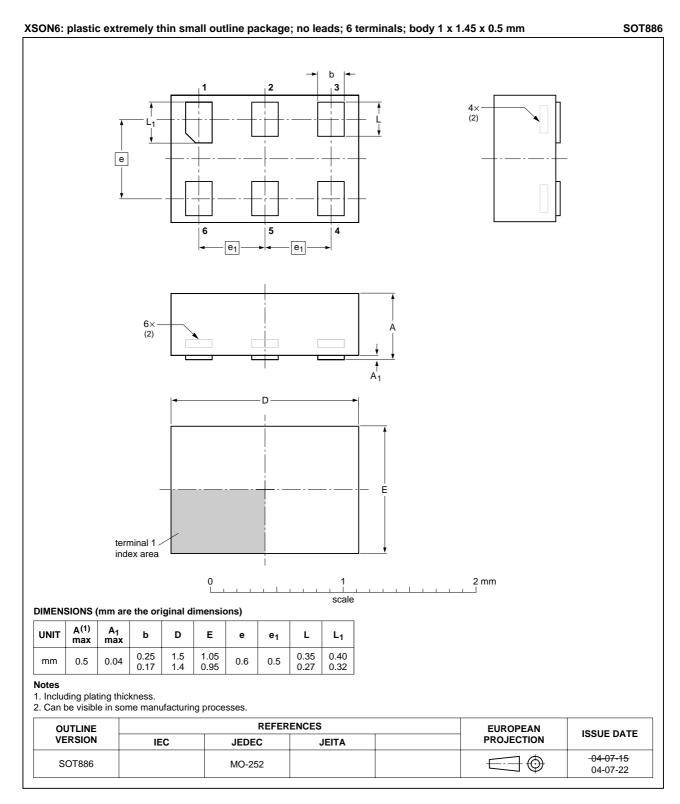


Fig 10. Package outline SOT886 (XSON6)

Low-power 2-input NAND gate (open drain)

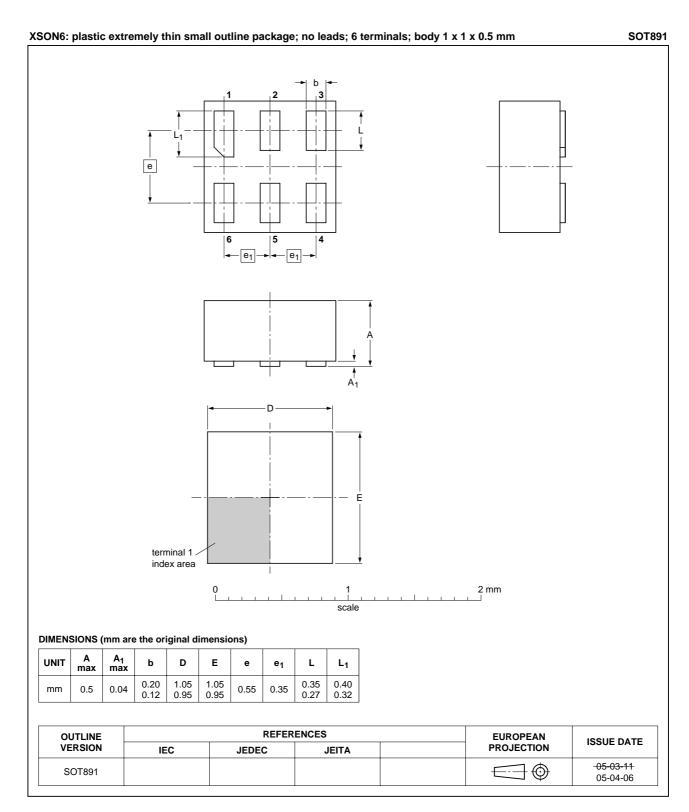


Fig 11. Package outline SOT891 (XSON6)

Low-power 2-input NAND gate (open drain)

## 14. Abbreviations

#### Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 15. Revision history

#### Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1G38_1	20061020	Product data sheet	-	-

#### Low-power 2-input NAND gate (open drain)

## 16. Legal information

#### 16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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